Integrated 10 GHz Beacon Transmitter

After the decline in use of ATV in Germany, an idea of building a 3 cm beacon at DB0HDF emerged. A survey of the equipment landscape revealed some shortcomings: Currently, no commercial all-in-one 10 GHz beacon transmitter is available. Documented designs exist, but often are built from a) many individual components (tin-can style) and/or b) obsolete and unavailable parts.

The goal of this project was building a 10 GHz beacon transmitter suitable for long-term unsupervised operation from commercially available integrated circuits. To make full use of the transmit power constraints in Germany, an output power of 1-2 W was targeted. Support for contemporary digital beacon transmission modes such as PI-4 was also a requirement for the design. Remote monitoring (telemetry) and control functionality was the third critical item on the feature list for a complete design.

Architecture

A simple block diagram of the beacon transmitter is shown in the figure below.

The beacon transmitter accepts an external 100 MHz reference clock provided by a GNSS-disciplined oscillator. GNSS stabilization is the de-facto standard for beacons on 10 GHz and above due to their narrow spacing and small bandwidth. It also enables receiving stations to use the beacon as a frequency reference for aligning their own equipment.

A Silicon Labs Si5342 is used as a crystal-driven reference PLL, which takes care of reference clock jitter cleaning and modulation generation. The high-resolution fractional divider allows synthesizing sub-Hz frequency steps of the output RF carrier, which are required for modern modulation formats. Due to the architecture of the synthesizer, no appreciable fractional spurs are generated in the process, yielding a very clean output spectrum with excellent phase noise. This IC generates in intermediate frequency of about 162 MHz, which is an integer multiplication factor lower than the final RF output frequency. A Linear LTC6948 RF PLL IC is used to multiply this signal by 16, up to a frequency of 2.592 GHz. From this point on, an Analog Devices HMC443 multiplier is used to create the final 10.368 GHz frequency. The multiplication creates some harmonic content at +-N*2.592 GHz away from the carrier, which are suppressed by a Mini-Circuits BFCN-Series MLCC bandpass filter. At this point, the final PA (Analog HMC952A) amplifies the signal up to around 1.5 W before reaching an SMA antenna connector.

The HMC952A also has a built-in output RF power detector, which is read out by an on-board microcontroller with integrated ADC. This simplifies the design since no external coupler is required to monitor forward power. The MCU further takes care of reading out the various DC power sensors on the board (to monitor voltages and currents of the SMPSes) and runs the sequencing of the beacon transmitter itself.

RF Design

One of the key design features that helps with driving down cost is working with a commercial four-layer FR4 stackup. These have become ubiquitous and cheap to use, so one supplier (JLCPCB from

China) was chosen and their PCB process characterized for RF performance. Two dedicated RF test coupons were designed: Based on the results of long simulations, prototype designs for SMA connector footprints, microstrip, coplanar waveguides etc were built.

The very thin two outer layer pairs can be used for RF traces (outer layer for signal, layer just below as a reference plane). Their biggest advantage is their narrow layer spacing (only about 150 µm), but is also the biggest complication: Successfully designing a well-performing PCB-to-SMA transition required lots of care (and simulation time): Achieving reflection-free coupling of the whole energy into connectors with large dielectric interfaces on the PCB side was not possible in a satisfactory manner. Finally, an SMA connector with a tapered dielectric interface was chosen (Amphenol 901-10511-2) and GCPWs were chosen for RF lines on the beacon PCB. With these connectors, very good return loss was achieved in both simulation and measurements, and the PCB process showed good performance at about 0.5 dB/cm of loss at 11 GHz at better than 30 dB return loss. The characterization report of the test coupon is available

here

Based on these results, the key RF components could be laid out. Since all components are internally matched reasonably well, no on-PCB matching was foreseen, except for an SMD attenuator between the RF PLL and the multiplier. This mostly improves harmonic content of the multiplier output by avoiding excessive overdrive, but also helps with input matching of course.

All RF traces carrying 10 GHz were kept as short as reasonably possible, a task made easier by the exclusive use of leadless SMD components (DFN, QFN ICs, SMD capacitors/resistors/filters).

Thermal/Power Design

Testing

Transmitter Integration at DB0HDF

Operations

References and Resources