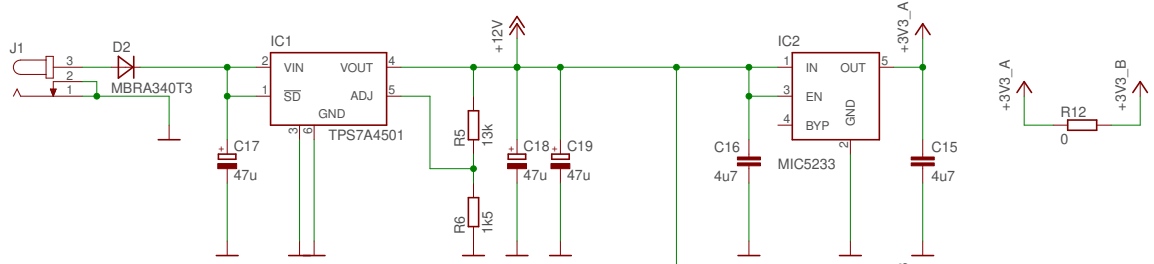
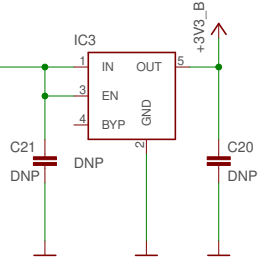
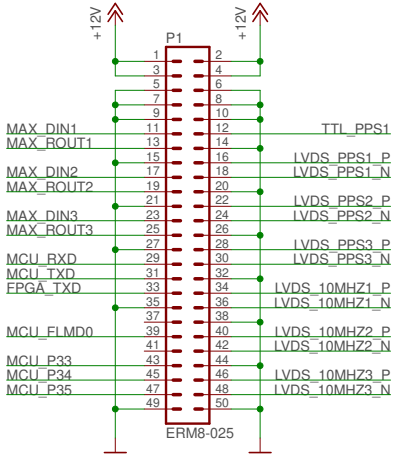


Vout = 1.21V * (1+R2/R1) + 3uA * R2
Vout(nom) = 11.74 V
Vdrop(I=1A, T=25°C) = 250 mV
Vdrop(I=0.3A, T=125°C) = 175 mV





Mounting holes are 4mm diameter.

Pinout from:
https://www.eevblog.com/forum/beginners/does-anyone-recognize-this-board-is-it-a-gpsdo/msg719301/#msg719301

NEC 10 MHz GPSDO Break Out Board

Design Stefan Biereigel 2018

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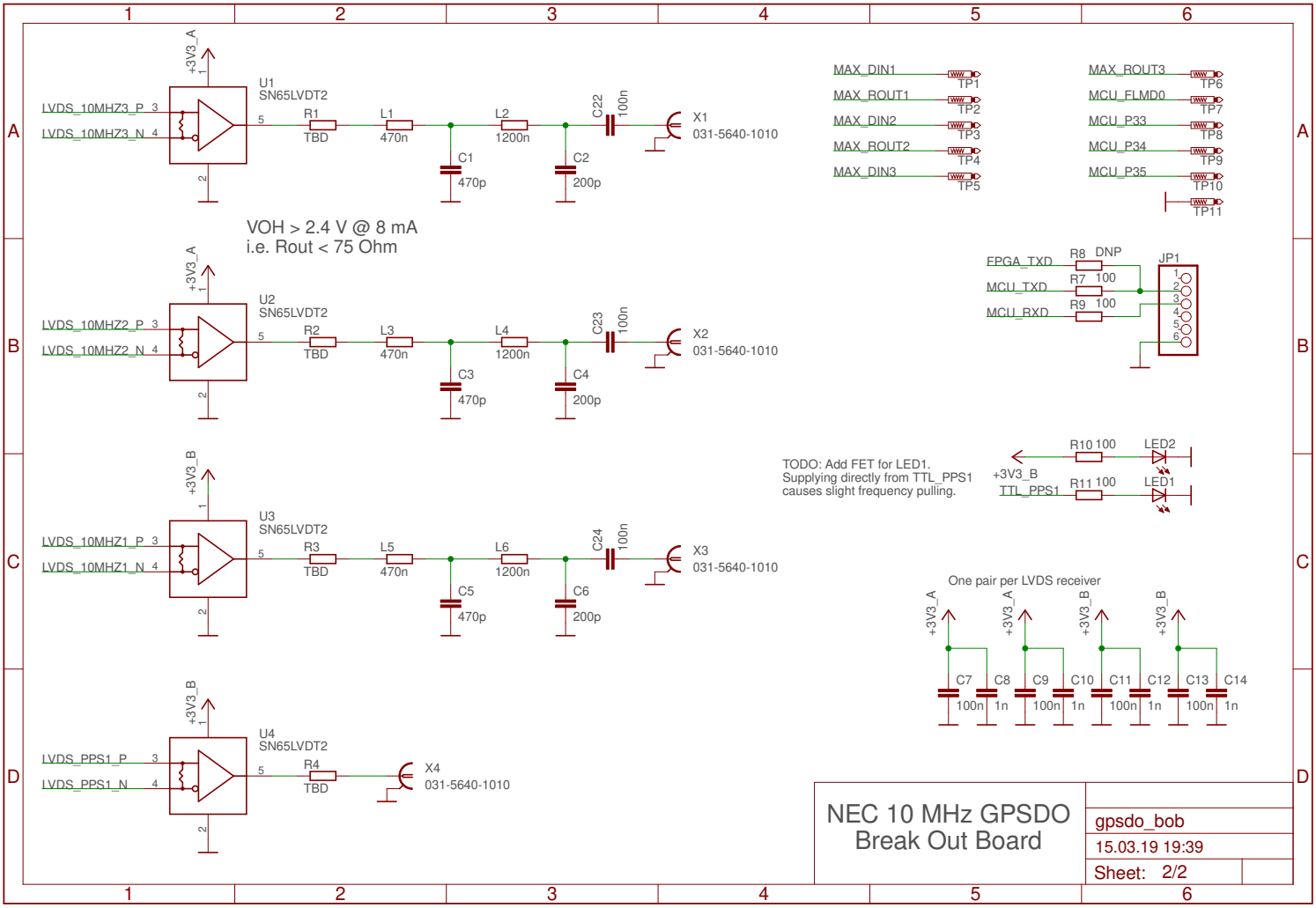
1
2
3
4
5
6
A
B
C
D
+3V3_A
U1
SN65LVDT2
LVDS_10MHZ3_P
LVDS_10MHZ3_N
R1
TBD
L1
470n
L2
1200n
C22
100n
X1
031-5640-1010
C1
470p
C2
200p
VOH > 2.4 V @ 8 mA
i.e. Rout < 75 Ohm
+3V3_A
U2
SN65LVDT2
LVDS_10MHZ2_P
LVDS_10MHZ2_N
R2
TBD
L3
470n
L4
1200n
C23
100n
X2
031-5640-1010
C3
470p
C4
200p
+3V3_B
U3
SN65LVDT2
LVDS_10MHZ1_P
LVDS_10MHZ1_N
R3
TBD
L5
470n
L6
1200n
C24
100n
X3
031-5640-1010
C5
470p
C6
200p
+3V3_B
U4
SN65LVDT2
LVDS_PPS1_P
LVDS_PPS1_N
R4
TBD
X4
031-5640-1010
MAX_DIN1
MAX_ROUT1
MAX_DIN2
MAX_ROUT2
MAX_DIN3
TP1
TP2
TP3
TP4
TP5
MAX_ROUT3
MCU_FLMD0
MCU_P33
MCU_P34
MCU_P35
TP6
TP7
TP8
TP9
TP10
TP11
FPGA_TXD
MCU_TXD
MCU_RXD
R8 DNP
R7 100
R9 100
JP1
TODO: Add FET for LED1.
Supplying directly from TTL_PPS1
causes slight frequency pulling.
+3V3_B
TTL_PPS1
R10 100
R11 100
LED2
LED1
One pair per LVDS receiver
+3V3_A
+3V3_A
+3V3_B
+3V3_B
C7 100n
C8 1n
C9 100n
C10 1n
C11 100n
C12 1n
C13 100n
C14 1n
NEC 10 MHz GPSDO
Break Out Board
gpsdo_bob
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